REMARKS

Claim 1 has been amended to recite that the substrate is formed of hexagonal crystal (support is found at page 3, lines 26-28 of the specification) and to more clearly recite the claimed line widths. Claims 1 and 2 have been amended to remove reference numbers specific to the drawings. Claim 3 has been amended to correct a typographical error. No new matter has been introduced. Entry and consideration of the amendments are respectfully requested.

Response to Rejection under 35 U.S.C. § 103

A. Claims 1, 3-7, 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over JP 10125958 to Shuji et al. ("Shuji") in view of U.S. Patent 4,604,161 to Araghi ("Araghi").

Regarding claim 1, Shuji was cited as teaching a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate, comprising: a step of linearly forming first grooves (11) in a desired chip shape by etching on a side of the gallium nitride compound semiconductor layers (2, 3) of said wafer ([0007], lines 1-6; Drawing 3, elements 11, 2, 3) and a step of dividing said wafer along said first and second grooves into pieces each of a chip shape ([0007], lines 11-12; [0010], lines 12-14; [0021], lines 9-10). The Examiner asserted that the wafers are separated along the "Chuo Line". Shuji is further cited as teaching a step of forming second grooves (22) having a nearly equal or smaller line width (W2) than a line width (W1) of the first grooves on a side of the substrate (1) of said wafer ([0007], lines 9-10; Drawing 3, elements W1, 11, W2, 22).

The Examiner recognized that Shuji does not teach a step of forming second grooves (22) having a nearly equal or smaller line width (W2) than a line width (WI) of the first grooves on a

side of the substrate (1) of said wafer at positions not conforming to the central lines of the first grooves. Araghi is cited as teaching a step of forming second grooves...of said wafer at positions not conforming to the central lines of the first grooves (column 3, lines 50-56; Fig. 3, elements 35, 37, 40, 44, 45).

The reason for combining the teaching of Araghi with the teaching of Shuji as asserted by the Examiner is to provide chips having precisely controlled ends and line edges for butting against the ends of like arrays.

Regarding claims 3-5, the Examiner recognized that Shuji in view of Araghi does not teach the claimed features but asserted that the subject features would have been obvious to a skilled artisan because "[w]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation" (citing *In re Aller*).

Applicant responds as follows.

First, Shuji teaches away from the offset center lines of Araghi. As shown, for example, in paragraphs [0012] and [0027], Shuji teaches a conventional method which enables the center lines of the first grooves to conform to the center lines of the second grooves (as shown in FIG. 4 of the Applicant's specification).[1] Applicant has prepared a translation of paragraphs [0012] and [0027] of Shuji (submitted herewith) and notes the following. The last sentence of paragraph [0012] of Shuji describes that "through the wafer is most preferably enabled to be cut straight at the points where the first grooves 11 agree with the center lines of the second grooves 22,

[1] As described under "Brief Description of the Drawings" at page 4, lines 20-21 of the specification, "Fig. 4 is a schematic cross-section of the wafer for illustrating the conventional method."

namely the positions denoted by a broken line a, as illustrated in FIG. 1." Shuji also teaches in paragraph [0027] that "The method of this invention for the production of gallium nitride-based compound semiconductor chips forms the first grooves so deeply as to penetrate the gallium nitride-based compound semiconductor layer and even remove a part of the sapphire substrate 1 as shown in the cross-section of FIG. 3. The method of this invention, therefore, enables the grooves to be cut straight at mutually coinciding positions by decreasing the cutting distance between the first grooves 11 and the second grooves 22." Further, Shuji teaches away from separating the chips along slanted lines since Shuji teaches that when the thickness of the wafer is too thick, the fracture line may become slanted as shown along line c in Drawing 1 ([0010]).

In contrast, Araghi teaches center lines which are deliberately offset so as to allow the tension of the crystalline plane of the related etched end groove to terminate near or adjacent the center line or middle portion of the inside groove (col. 3, lines 50-56).

Accordingly, modifying Shuji so as to offset the opposing grooves thereby allowing the wafer to be fractured along a diagonal plane renders Shuji unsatisfactory for its intended purpose. That is, Shuji teaches away from combination with Araghi.

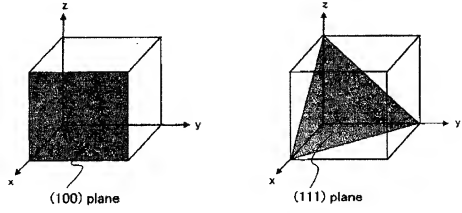
Second, a skilled artisan would not have been motivated to precisely control the ends and line edges of Shuji for butting against the ends of arrays as in Araghi. Araghi teaches abutting chips in order to provide high resolution sensor arrays without image loss or distortion at the array junctions (col. 1, line 66 to col. 2, line 4). In contrast, Shuji teaches light emitting devices which are not abutted in the manner of Araghi. Accordingly, a skilled artisan would not have been motivated to abut the light emitting devices of Shuji as asserted by the Examiner.

Third, with regard to claim 6, the Examiner's interpretation is incorrect. The first grooves taught by Shuji are so deeply formed as to penetrate the gallium nitride-based compound

semiconductor layer and remove a part of the sapphire substrate 1 (paragraph 0027, FIG. 3). Then, the V-shaped grooves 35 taught by Araghi are formed by removing a part of the wafer 20 (column 3, lines 36-41, FIG. 3). The Examiner's interpretation purporting that "First grooves are formed in material layers comprising gallium nitride layer 3 over which an electrode-forming surface can be formed" (Office Action, page 2, last line -page 3, first line), therefore, is incorrect. Accordingly, a skilled artisan would not have achieved the features of claim 6 based on the disclosures of Shuji and Araghi, contrary to the Examiner's assertion.

Fourth, the substrate of Shuji and the substrate of Araghi differ substantially. Shuji teaches a sapphire substrate ([0001]) while Araghi teaches a silicon substrate (col. 3, lines 16-17). The sapphire substrate disclosed by Shuji is a hexagonal crystal, namely a material which possesses no cleavability and allows no easy cutting (Shuji, paragraph [0005]). In contrast, the silicon substrate disclosed by Araghi is a cubic crystal, namely a material which possesses the property of cleaving in the (111) plane. It is disclosed in Araghi at column 3, line 50 to column 4, line 5 that the chips 10 are separated from the wafer 20 by utilizing the aforementioned property thereby cleaving the silicon substrate in the (111) plane. Applicant provides below a schematic representation of the referenced plane:

Fig. 1 Crystal Plane of Cubic Structure



It is impossible to combine the method of Araghi, which separates chips by utilizing the cleavability of silicon crystal, with the method of Shuji, which utilizes a sapphire substrate possessing no cleavability.

Fifth, with regard to claim 4, Applicant disputes that Shuji in view of Araghi disclose the general conditions of the rejected claims, as asserted by the Examiner. On pages 3-4 of the Office Action, the Examiner asserted that "[w]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." The Examiner concluded that the subject matter of claim 4 would have been obvious to a person skilled in the art at the time of filing the invention of this application.

Rather, Araghi teaches that a chip 10 is fabricated from wafer 20 of silicon (column 3, lines 16-17) and that this chip 10 is separated in the (111) plane 37, which is the cleaving plane of the silicon substrate. The difference between the (100) plane and the (111) plane of a silicon substrate are shown in the diagram above. The angle that is formed between these two planes can be found by a geometric calculation to be 54.7°.

Further, amended claim 1 recites that the claimed substrate is formed of hexagonal crystal. The claimed crystal differs in crystal structure from the silicon substrate disclosed by Araghi. Further, the substrate of the invention of this application does not possess the same cleavability as the silicon substrate.

Accordingly, a skilled artisan would not have achieved the features of claim 4 based on Shuji and Araghi and the conditions disclosed therein by routine experimentation, contrary to the Examiner's assertion.

Reconsideration and withdrawal of the rejection are respectfully requested.

B. Claims 1 and 2 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Shuji in view of Araghi as applied to claim 1 above, and further in view of U.S. Patent Application Publication 2002/0014681 Al to Tsuda et al.

Claims 1 and 2 are patentable over Shuji in view of Araghi and Tsuda at least for the reasons cited above. Namely, Shuji teaches away from the offset center lines of Araghi; a skilled artisan would not have been motivated to precisely control the ends and line edges of Shuji for butting against the ends of arrays as in Araghi; the Examiner misinterpreted claim 6; the substrate of Shuji and the substrate of Araghi differ substantially; and Shuji in view of Araghi does not disclose the general conditions of the rejected claims. In this regard, Tsuda does not cure the deficiencies of Araghi and Tsuda.

Further, with regard to claim 2, the Examiner has given no explanation as to which of the grooves disclosed in Tsuda correspond to the first grooves or the second grooves of claim 1.

Also, the first grooves in claim 2 of this application are formed on the same surface (the surface parallel to the principal surface of the substrate) along two mutually orthogonal directions. Then, the second grooves in claim 2 of this application are formed on the surface of the opposite side of the side of the substrate on which the first grooves are formed in two mutually orthogonal directions.

In contrast, Tsuda do not disclose the formation of grooves on each of both surfaces of a substrate in two mutually orthogonal directions.

Reconsideration and withdrawal of the rejection are respectfully requested.

C. Claims 1 and 8-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Shuji in view of Araghi as applied to claim 1 above, and further in view of U.S. Patent Application Publication 2001/0038655 Al to Tanaka et al.

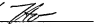
Claims 1 and 8-10 are patentable over Shuji in view of Araghi and Tanaka at least for the reasons cited above. Namely, Shuji teaches away from the offset center lines of Araghi; a skilled artisan would not have been motivated to precisely control the ends and line edges of Shuji for butting against the ends of arrays as in Araghi; the Examiner misinterpreted claim 6; the substrate of Shuji and the substrate of Araghi differ substantially; and Shuji in view of Araghi does not disclose the general conditions of the rejected claims. In this regard, Tanaka does not cure the deficiencies of Araghi and Tsuda.

Reconsideration and withdrawal of the rejection are respectfully requested.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Translation of Paragraphs [0012] and [0027] of JP 10-125958 to Shuji et al.

(Paragraph 0012)

"[Function] The operation of the method of production of this invention will be explained based on the drawings, ie FIG. 1 to FIG. 4 which show a process for cutting a wafer into chips. FIG.3, however, shows a process for cutting a wafer into chips by the method of a working example of this invention. FIG. 1 is a type section of the wafer that has an n-type nitride semiconductor layer 2 (n-type layer) and a p-type nitride semiconductor layer 3 (p-type layer) laminated on a sapphire substrate 1. The wafer is depicted in a state such that the first grooves 11 are linearly formed in prescribed chip shapes on the nitride semiconductor layers' side of the wafer and further second grooves 22 having a narrower line width than the line width of the first grooves are formed at the positions agreeing with the center lines of the first grooves 11. As depicted in this drawing, however, the first grooves are formed by etching the p-type layer 3 so as to expose the n-type layer 2 and the second grooves are formed by scribing. Though the wafer is most preferably enabled to be cut straight at the points where the first grooves 11 agree with the center lines of the second grooves 22, namely the positions denoted by a broken line a, as illustrated in FIG. 1, the cutting positions will not reach the p-n junction interface and defective chips will not occur even if the cutting lines are curved as denoted by a broken line b because a line width W1 of the first grooves 11 is greater than a line width W2 of the second grooves 22."

(Paragraph 0027)

"The methods of the foregoing comparative examples 1 - 5 form the first grooves in such a state as to avoid penetrating the gallium nitride-based compound semiconductor layer as shown in FIG, 1 or FIG. 2. The method of this invention for the production of gallium nitride-based compound semiconductor chips forms the first grooves so deeply as to penetrate the gallium nitride-based compound semiconductor layer and even remove a part of the sapphire substrate 1 as shown in the cross-section of FIG. 3. The method of this invention, therefore, enables the grooves to be cut straight at mutually coinciding positions by decreasing the cutting distance between the first grooves 11 and the second grooves 22. Particularly, the wafer which is provided with the first grooves and the second grooves is enabled to be separated into a multitude of chips by being lightly pressed with a roller on the sapphire substrate side."